Chapter 1 Semiconductors and materials Area

RELIABILITY OF FLEXIBLE AMORPHOUS IN-GA-ZN-O (A-IGZO) THIN-FILM TRANSISTORS

Isai S. Hernandez-Luna[1], Pablo Toledo[2], Francisco Hernandez-Cuevas[1], Norberto Hernandez-Como[1*]

[1]Centro de Nanociencias y Micro y Nanotecnologías, Instituto Politécnico Nacional, Mexico City, Mexico.

[2]Escuela Superior de Ingeniería Química e Industrias Extractivas, Instituto Politécnico Nacional, Mexico.

nohernandezc@ipn.mx

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Abstract

The application of flexible electronics will require a new class of electronic devices and systems with outstanding characteristics such as lightness and mechanical flexibility, giving the possibility of gradually entering in the daily people lives as human health monitors. Amorphous oxide semiconductors have been part of this type of application, becoming attractive materials for new generation flexible electronics. In this work we evaluate the scalability of our thin-film transistor technology for possible applications such as health monitors. The characterization of two identical TFT device fabrication processes is explored with the variant of being fabricated on two different substrates, rigid and flexible. Rigid substrate TFTs show slightly higher initial characteristics compared to flexible TFTs. The degradation in flexible devices is attributed to constant mechanical stress and roughness of the flexible substrate. Finally, in flexible devices under conditions of mechanical stress with a radius of curvature of 4 mm, present a combined behavior of a flexible device without mechanical stress to a device fabricate on a rigid substrate.

Keywords: flexible electronics, oxide TFT, InGaZnO (IGZO); compatible devices, reliability

1. Introduction

The growing demand for electronics with innovative features has recently oriented exploration towards new lines of technological research [1 – 4]. With features such as light weight, low cost, adaptability, and ease of use, flexible electronics have been a topic of special interest in the scientific research community in recent decades [4, 5]. In this sense, flexible electronics, which consists of devices and systems capable of displaying electrical functionality while mechanical stress is applied, has shown great promise in many practical applications, such as wearable devices, smart implants, folding screens, physiological monitoring, among many [6 – 9]. Similarly, thin-film electronics based on oxide semiconductors have recently attracted increasing interest due to the characteristics they share with flexible substrates [10 – 14]. This combination of properties, enabled using advanced materials and processes, has find the way for new applications in different fields, such as detection technologies and healthcare systems [15]. As active devices in such flexible systems, the reliability of oxide semiconductor thin-film transistors is a subject of study, which must withstand the combined stress of electrical and mechanical loads.

Since the use of amorphous metal oxides such as indium-gallium-zinc oxide, a-IGZO as the semiconductor material, or active layer, in thin-film transistors (TFTs) was shown by Nomura et al in 2004 [14], a huge effort has been put into the research of amorphous oxide semiconductor (AOS) TFT devices, especially for their application in new generation flat panel displays (FPDs) and now in alternative applications [16, 17]. Among the main advantages of amorphous semiconductor oxide materials are that it is possible to obtain them using conventional deposition methods, such as sputtering, pulsed laser, by atomic layers, even at room temperature [14, 18, 19]; in addition, its amorphous structure allows to maintain similar properties in devices fabricated even in large areas [20].

The characteristics of amorphous semiconductor oxides are mainly attributed to their electronic configuration, which presents a spherical symmetry of orbitals of their S-type energy sublevels, allowing a high degree of overlap between neighboring orbitals, forming a conduction path of free electrons despite its amorphous structure. Inherent to the material, there is the creation of oxygen vacancies, which affect the electrical properties of AOS [21, 22].

Regarding the electrical performance of AOS-based TFTs, the high field effect mobility observed with respect to hydrogenated amorphous silicon TFTs

(a-Si;H) or organic TFTs stands out, obtaining values around of 10 Vs, even if the AOS are processed at room temperature (RT), as well as good stability under polarization and lighting stress. The mentioned characteristics depend not only on the use of the semiconductor material, but also on the gate dielectric and the contact metal or metals within the TFT structure. Research on optimizing the cationic composition of compounds in semiconductor materials has been highlighted, as well as the variation in the methods used for their deposit, heat treatments after their deposit or at the end of transistor fabricated. In the use of dielectric materials, it is desired that they have dielectric constants higher than SiO_2, low leakage current, and good thermal stability. Additionally, the formation of an ohmic contact is essential for the fabrication of TFTs, in the drain and source regions have a significant influence on the performance of the device [23, 24].

The structure of the TFT can be coplanar or staggered type and bottom or top gate, depending on the position of the gate with respect to the semiconductor oxide. The coplanar structure generally means that the source/drain electrodes and the semiconductor material are in the same plane. The staggered configuration means that the metal electrodes and the semiconductor material are not in the same plane, but rather are interleaved. For sensor applications, the bottom gate structure is generally used, allowing semiconductor material to act as an active layer to the outside environment. In the application of the TFT as a sensor, there are other configurations such as the case of the extended gate TFT, where the gate metal is used to sense the medium and have less contact resistance [25].

A TFT is used as a three-terminal device to connect to an external circuit that acts as an electrical signal amplifier or switch. The transistor is the central device for data processing and transmission. The three electrodes of the transistors are gate, source, and drain, and their three positions are not fixed and can be adjusted according to different processes to prepare different device structures. Thin Film Transistors (TFTs) are recognized as key building blocks/tools for the implementation of electronic logic circuits.

The use of polyimide (PI) in the industry is the most widely used representative plastic substrate presenting excellent thermal, chemical, and mechanical resistance. PI substrates withstand the fabrication process of Low Temperature Polycrystalline Silicon (LTPS) TFTs and oxide semiconductor TFTs [26]. Parallel to this, PI allows high uniform and achieve device functionality under different mechanical conditions, it is crucial to establish fabrication protocols to support electronic functionality under different types of deformation, such as bending,

stretching, creasing [27]. When a device is bent, the force applied to the device varies depending on the direction of bending and the radius of curvature. Depending on the magnitude of the force applied to the device, defects and dislocations can form in the active layer, leading to cracks from the gate electrode to the PI substrate in severe cases. This non-ideal phenomenon leads to deterioration of the electrical characteristics and reliability of TFTs.

The strategy that is taken is the fabrication of devices in two different substrates, rigid and flexible to aim at the scalability of the device for large area systems and flexible electronics. Furthermore, the transistors are characterized to evaluate their functionality as sensor conditioning circuits for portable devices, and health devices. By proper design of the device structure, is possible to reduce the effect of mechanical deformation on the active layer, allowing the realization of highly deformable transistors.

2. Experimental part

Two fabrication processes of IGZO TFTs were carried out, A and B samples, the difference between the processes lies in the use of different substrates as mechanical support for devices. In process A, a square-shaped Corning Eagle XG, one inch per side and 0.7 mm thick, purchased by Corning Incorporated, is occupied, with the characteristic of being occupied up to 600 °C. For process B, a Kapton HN Polyimide (Pi) substrate with a square shape, two inches per side and 50 μm thick, purchased from DuPont, was used. Pi has the characteristic of being used up to 400 °C. For the use of Pi, a dehydration heat treatment was carried out in air at 300 °C for 1 h, this to prevent expanding or contracting during processing. The flexible substrate is supported throughout the fabrication process on a glass support using the surface tension provided by a few drops of water. Both substrates were cleaned with acetone, alcohol, and water in an ultrasonic bath, prior to use.

The fabricated structure of the TFTs for both samples is bottom gate and staggered type. To define the bottom gate electrode in process A, we use Cr/Au as bilayer with 10/50 nm of thickness, the electrode was deposited using the electron beam evaporation technique and defined by wet etching based on ceric ammonium nitrate/potassium iodide. In process B, we use aluminum (Al) with 150 nm of thickness deposited by thermal evaporation and defined with a

phosphoric acid solution. The difference between the gate metals is due to the possibility of Pi attack on the solutions that define the Cr/Au metals.

For both processes A and B, 22 nm of Al_2O_3 was used as the dielectric layer deposited by atomic layer deposition (ALD) at 150 °C, using trimethylaluminum (TMA) and H_2O as precursors. Afterwards, 15 nm of IGZO layer was deposited by sputtering at room temperature at 70 W in an argon plasma. HCl and BOE 6:1 was used to define the semiconductor and gate dielectric layers, respectively. Subsequently, 150 nm Al were deposited by sputtering as source and drain electrodes with 150 W in argon plasma. The definition of the drain and source metal is carried out through the Lift-off process to avoid possible deterioration of the top part of the semiconductor material. Finally, for both processes, 200 nm of polymethylmethacrylate (PMMA) was deposited by spin-coating as a passivation layer with a heat treatment at 150 °C in air. The definition of PMMA is carried out using the RIE in an oxygen environment with a power of 130 W.

We use lithography processes to define the areas that make up the TFT structure, these processes were carried out using the direct writing technique using a Heidelberg DWL66FS system and positive photoresist at 115 °C. The photoresist development process is carried out with a potassium hydroxide-based solution at room temperature. In the figure 1a) we show the bottom gate structure in staggered configuration of the fabricated TFT and b) optical microscope image of the completed device.

a) b)

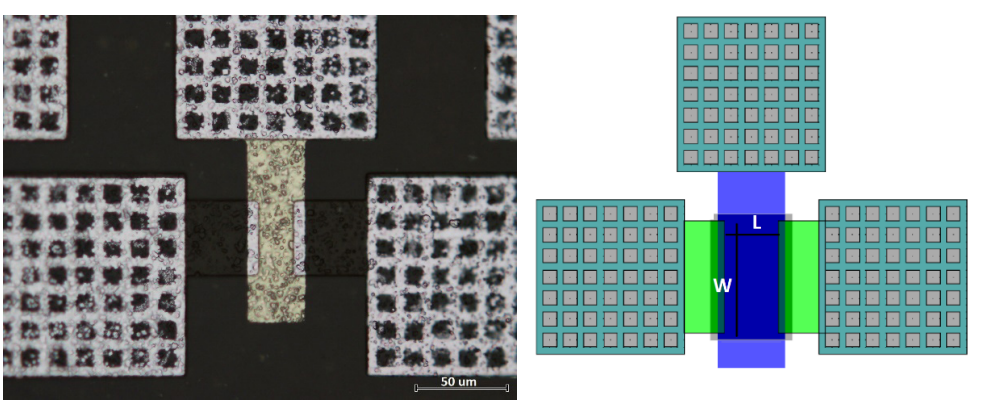

Figure 1. a) Shows the bottom gate structure in staggered configuration of the fabricated TFT and b) optical microscope image of the completed device.

The fabricated TFTs have two channel widths of 80 μm and 160 μm with two different channel lengths of 40 and 80 μm. In addition to the transistors, metal insulating metal (MIM) capacitors with dimensions of 80x80 μm per side were fabricated. Electrical characterization was performed with a Keithley 4200-SCS system at room temperature.

3. Results and discussion

According to the C-V characterization of MIM capacitors, the dielectric constant of Al_2O_3 was extracted, ki=6.4, this value is constant for the samples A (S-A) and B (S-B). Figure 2 shows the linear and saturation transference curves of a sample device A, measured at V_{DS}= 0.1 V and V_{DS}=5 V, correspondingly. A transistor with W=160 μm and L=40 μm is occupied. From the curves, the field effect mobility in the saturation region (μFET) of the transistor are extracted, μ_{FET}=11 cm^2/Vs, threshold voltage (V_{th}), V_{th}=0.84 V, both extracted from the linear fit of the graph IDS1/2 vs. VGS, according to the IDS formula in saturation [28]; Delta Vth (DV_{th}), which corresponds to the voltage window formed by measuring the negative to positive and reverse voltage, DVth=0.1V, the Ion/Ioff ratio of the transistor in the saturation transference curve, I_{ON}/I_{OFF}=6.8x10^7 and the subthreshold slope (SS), corresponds to the increase in V_{GS} necessary to increase the I_{DS} in a decade, SS=256 mV. The gate current (I_{GS}) is plotted which is below 10 nA.

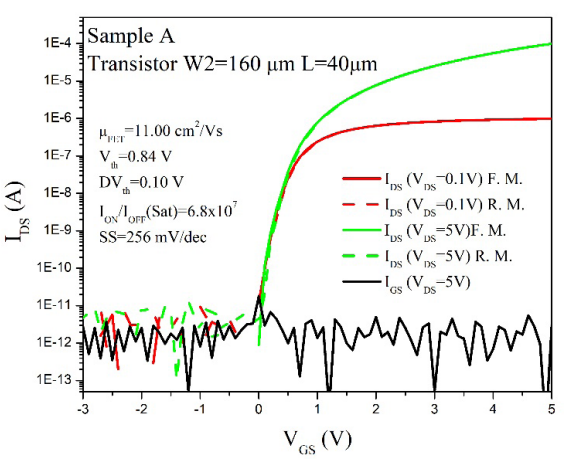

Figure 2. Shows the linear and saturation transference curves of a sample device A, with forward (F.M.) and reverse (R.M.) measurements.

In Figure 3a, the output characteristics of two devices with the same channel length L=40 μm and different channel width are shown, W1=80 μm and W2=160 μm. We can observe that I_{DS} with respect to its geometric relationship, there is a good coincidence of all the output characteristic curves, this indicates a good repeatability of the devices within the fabrication process. Figure 3b graphs the transference in saturation for four different devices, a good fit between them can be observed.

a) b)

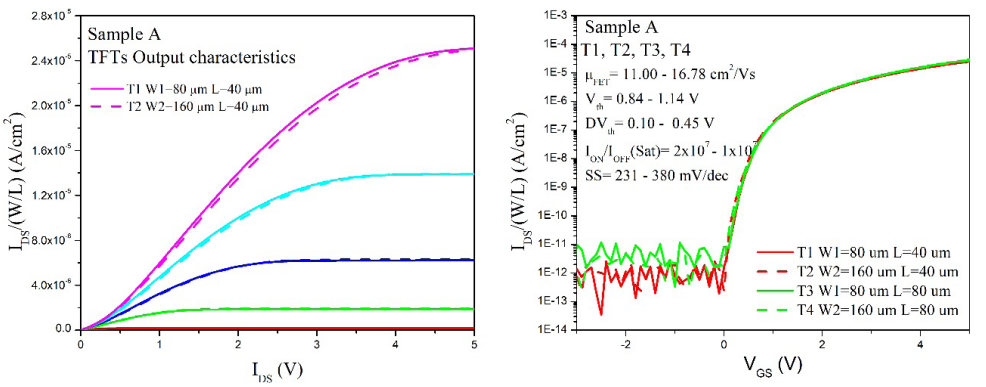

Figure 3. Show a) output characteristics and b) transfer curves for a device of sample A.

Figure 4 shows the linear and saturation transference graphs for a sample B device, measured in a flat state, occupying a rigid glass substrate as a support. The device presents a reduction of μ_{FET}=8.9 cm^2/Vs, a reduction in Vth and an increase in the value of SS with respect to the device of sample A. The values of the DV_{th} window for both sets of curves, the current gate and the I_{on}/I_{off} ratio of the transistor hold with respect to the device in sample A.

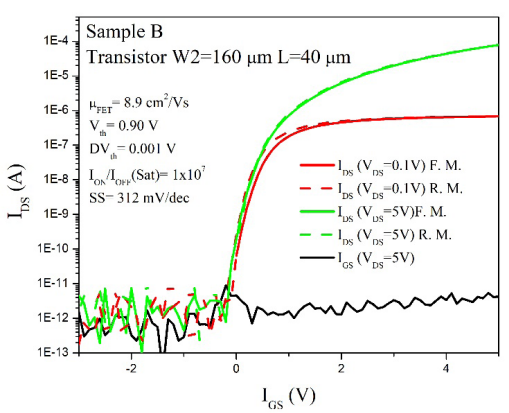

Figure 4. Shows the linear and saturation transference curves of a sample device A.

Figure 5 shows the graphs of the comparison of sample A and B for a device with the same geometric configuration. We can observe a slight reduction in the drain current for sample B. Figure 5a, shows an increase on origin resistor (Origin R) at V_{GS}=5 V for sample B. In figure 5b a reduction of the drain current is shown for sample B, the DV_{th} windows are kept in the same range of values. A general reduction of the drain current of around 15 to 20 % can be observed in sample B compared to sample A. This may be due to the roughness of the flexible substrate and the constant flexing that the substrate exhibited during the fabrication process.

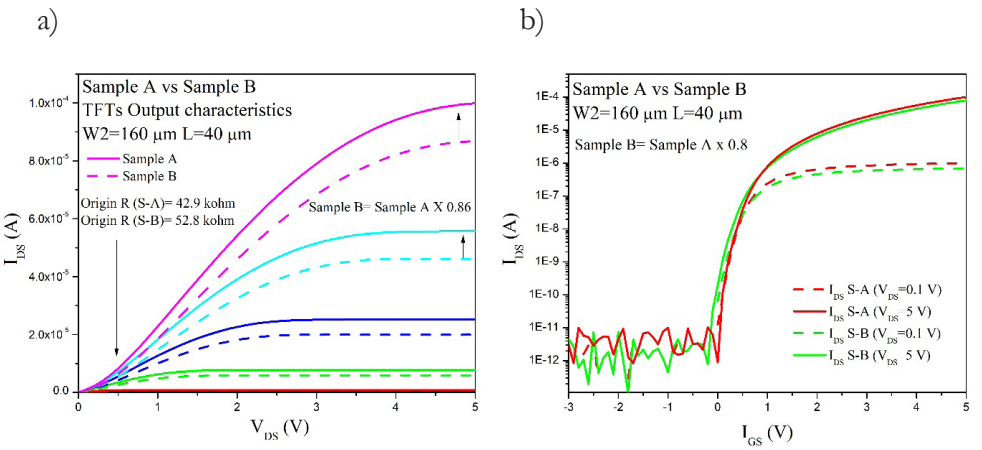

Figure 5. Shows the comparison of the a) output characteristics and b) transfer curves for devices of sample A and B without mechanical stress.

Figure 6 shows the transference curves for a device from sample B under conditions of mechanical stress with a bending radius of 4 mm. The device is completely new, which indicates that it has not been subjected to prior electrical characterization. A slight increase in field effect mobility is presented, and a reduction in V_{th} compared to a device without flexion. The values of SS, I_{ON}/I_{OFF} and I_{GS} are kept in close range for flexible devices. There is a slight increase in the DV_{TH} window for the linear transference curve, but not significant for the saturation transference curve.

Figure 7a shows the comparison of the saturation transference curves for a device from samples A, B and B with flexion of 4 mm radius. A clear shift of V_{th} towards negative values and an increase in ID_{max} current is observed for device B with flexion with respect to the device of sample A. The I_{GS} of the devices is plotted, where no notable variation is shown. Figure 7b shows the output characteristic curve for a value of V_{GS}=5 V, it highlights the behavior of devices B with

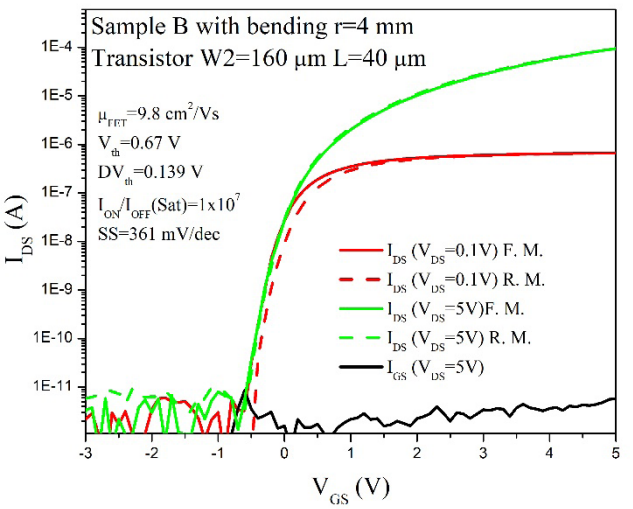

Figure 6. Show the transfer curves for a device of sample B with mechanical stress with a bending radius of 4 mm.

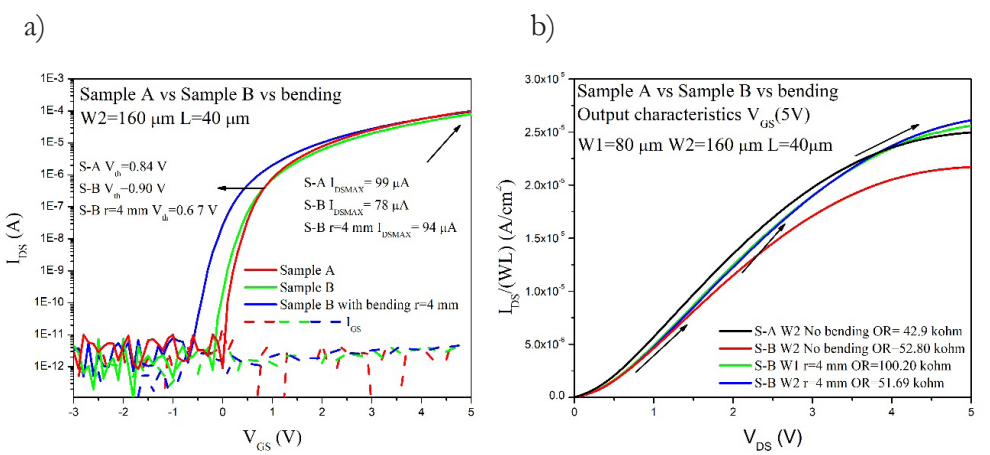

Figure 7. a) Transfer curves and b) output characteristics for devices of sample A, B, and B with bending

bending, which have an initial behavior corresponding to a flexible device without mechanical tension to a behavior of a device fabricated on a rigid substrate.

When comparing the results of two samples fabricated with the same technology, but changing their mechanical support, a reliability of the manufacturing process was obtained by seeing a good repeatability in their characteristic curves. For flexible substrates that show mechanical stress conditions with a radius of curvature of 4 mm, we can predict their use as health monitors in portable

applications that at least have a radius of curvature greater than 4 mm, for example the human finger has a radius of curvature of 12 mm, which may be feasible to use in this kind of applications.

4. Conclusions

In this work we evaluate the scalability of our thin-film transistor of fabrication process, when comparing the characterization of two identical TFT devices with the variant of being fabricated on two different substrates, rigid and flexible. Rigid substrate TFTs show slightly higher initial characteristics compared to flexible TFTs. The degradation in flexible devices is attributed to constant mechanical stress and roughness of the flexible substrate. Finally, in flexible devices under conditions of mechanical stress with a radius of curvature of 4 mm, present a combined behavior of a flexible device without mechanical stress to a device fabricate on a rigid substrate. We consider the use of this fabrication process for possible applications such as portable health monitors.

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